A new FPGA and multi-core processor architecture for high-performance signal processing and control systems

Tenova I2S’ technology for high-performance signal processing and control systems gives unparalleled performance by implementing the systems’ real-time algorithms, processes and computations directly within a unified framework of generic programmable hardware (field programmable gate arrays), overseen by a real-time operating system supervisor. The systems’ many components and interconnections are each realised by identical hardware components (building block style), thereby allowing a single form of spare hardware to support the many possible system arrangements.

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Automatic gauge control (AGC) and strip thickness measurement (STM) are two critically important activities in the cold reduction of flat strip. Over the past 30 or so years, Tenova I2S (formerly Integrated Industrial Systems, Inc. [I2S]), has supplied more than 240 AGC systems and more than 510 non-contact, radiation transmission-based STM systems (both isotope and X-ray) worldwide, starting with one of the first microprocessor controlled (Z80-based) AGC and STM systems in 1980.

Over the years, we have seen hardware/software technologies and their availabilities change radically, followed closely by the evolving needs of our customers; tighter tolerances, increased reporting and expanded interconnections between the mill’s systems, including a wide range of plant-wide customer-provided networks and computer systems. A great many hardware/software platforms and technologies have been employed to implement AGC and STM systems, ranging from commercially available equipment to highly specialised, custom/proprietary arrangements.

The past decade has seen various general purpose, commercial-off-the-shelf (COTS) technologies and philosophies take hold. COTS have now become a fixture in the marketplace. COTS equipment is developed for, and directed towards, a broad spectrum, high-volume market, whose needs and capabilities may or may not be suitably aligned with the requirements of high-performance AGC and STM system applications.

Essentially AGC and STM system suppliers are left to decide whether their product lines would be fashioned to address the high-performance needs of their narrowly intended application (and thereby consciously continue to employ certain amounts of proprietary equipment) or would consciously accept potential performance degradations to embrace a more market-attractive COTS-based system.

Interestingly, the rapid pace of commercial hardware development and quick product end-of-life obsolescence, is a mainstay in the unstable computer and electronics industries. It was not uncommon for newly marketed components/equipment to become obsolete and unsupported within 12-18 months of their initial unveiling. This can cause many COTS-based AGC and STM product lines to have the appearance of a patchwork quilt of ever changing hardware components and supporting software drivers with every new system incarnation being incompatible with effectively identical systems provided a year or two earlier.

These computer industry facts-of-life led many equipment providers to continue to develop and employ dedicated, proprietary hardware in certain specific facets of their systems. We have been among them.

In the past few years, however, a new COTS-based alternative has presented itself, which does not constrain the resulting system with a manufacturer’s preconceived views of what hardware arrangements and data flow architectures will be provided or not provided.

This alternative offers a general purpose programmable hardware environment through which software-based control signal processing and data flows can be implemented with ease. The same COTS-based alternative supports hard, real-time control and operating system software to assure deterministic responses to real-world events and conditions. Furthermore, all standardised network interfaces are supported, allowing a broad spectrum of commercial HMI software packages (often selected/directed by the customer) to be employed. It is very welcome news.
from simple logic to complex mathematical sequences and pipelined processing arrangements.

The hardware’s signal/logic interconnections and routings are defined by software schematics, block structured functions, procedural codes and/or hardware description language (HDL). When the code is compiled and downloaded to the target FPGA, the result is a true hardware implementation of the application.

The software configured/programmed hardware operates in a truly parallel nature without processor bottlenecks or execution sequence restrictions. The hardware sub-systems operate with complete independence at extremely fast execution rates (parallel operations at 40MHz clock speeds). Essentially, this is real-time, hardware multi-tasking.

**Fig 1** provides an illustration of the internal components/architecture of a typical FPGA integrated circuit.

Complex, real-time, closed-loop servo controls and signal processing, previously implemented only with discrete components or within real-time software environments, can now be completely implemented in this single-chip hardware. This HIL concept is shown in **Figure 2**.

The fact that the hardware is field-programmable means that flexibility and future expandability is ensured. Formerly, proprietary hardware and software are now replaced with programmed, general purpose commercial hardware, programmed via a commercial, open-architecture development language (eg, National Instruments LabView). The program for the FPGA is downloaded to the chip on system power-up, so updates are as simple as copying a file. Furthermore, identical commercial boards containing the FPGAs, can be placed in the same computer and independently programmed with completely different hardware applications. This means that a single, commercial hardware component will support the entire needs of the intended application, requiring only a single spare.

**NEW TECHNOLOGIES AND INNOVATIVE CAPABILITIES**

Two new technologies have become viable candidates for consideration in AGC and STM applications. They offer:

- General purpose, software programmed hardware arrangements.
- Closed-loop control, signal processing and data flows, all implemented in high-speed hardware (hardware-in-the-loop: HIL).
- Complete mathematics support directly implemented in the hardware.
- Support of hard, real-time control and real-time operating system software.
- Strict deterministic responses to real-world events and conditions.
- Simultaneous support of multiple operating systems and parallel processing.
- Standardised network interfaces and databases.
- Broad spectrum of commercial HMI software packages (often selected/directed by the end-user).

**Field programmable gate arrays (FPGA)** This new programmable hardware technology gives the ability to implement application-optimised hardware with the flexibility of programming. Integrated, single-chip circuits containing millions of programmable gates can be configured and interconnected for any need, ranging

**Multi-core processors** The recent release of multi-core CPUs (eg, Intel® Core™ 2 Duo processors) offer some

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![Fig 1 FPGA internal architecture and component arrangement](image1.png)

![Fig 2 Typical HIL closed-loop digital control application](image2.png)
very interesting opportunities to consolidate multiple system responsibilities in a single computer. These multi-core systems contain two identical processors on a single integrated circuit. The processors operate separately and are fully capable of supporting two completely independent operating systems (e.g., real-time VxWorks on one, Windows on the other) and functioning in a completely parallel arrangement. This offers a whole new dimension in modularity, flexibility and opportunities.

**SYSTEM ARCHITECTURES AND IMPLEMENTATIONS**

**AGC system** The Tenova I2S AGC system is a self-contained gauge control system capable of operating in a standalone arrangement or as a key participant in a fully integrated mill control system provided by Tenova I2S or another automation supplier. It is fully networkable and has a high degree of interface via an internationally standardised, onboard open connectivity (OPC) server. Figure 3 provides a block diagram illustration of the system architecture.

The primary components are:

- **AGC controller** This provides the real-time AGC functions, algorithm computations, roll force cylinder servo controls, gauging system interface, critical strip length/speed measurements and high frequency data acquisition for SPC analysis, reporting and general data acquisition (often coupled with intermediate bus architecture (IBA) data logging systems). The mill equipment interfaces and direct servo controls are provided by two FPGA-based subsystems that operate as intelligent, fully autonomous I/O and servo systems beneath a real-time operating system layer that executes within an independent core of the Intel® Core™ 2 Duo Processor. Real-time layer activities are performed by the National Instruments Real-Time LabView ETS software system (executing on a VxWorks Real-Time operating system supporting symmetric multiprocessing for the Core 2 Duo processor). Interfaces to the other control system computers (PLC, HMI, drive system) provide a Gigabit class Ethernet network interface and through the OPC Server executing on the other core.

- **Supervisory and HMI** This serves as the supervisor of the AGC controller, provides the primary interactive, graphical user interface HMI screens that support the Tenova I2S AGC system, and supports an internationally standardised OPC server. This Windows XP Pro operating system based component executes on the other independent core of the Intel® Core™ 2 Duo processor.

**STM systems** The Tenova I2S STM systems are based on transmission mode, radiation absorption/attenuation based, non-contact thickness measurement, employing isotope or X-Ray generated radiation. These are fully self-contained and capable of operating in a standalone arrangement or acting as a key participant in a fully integrated mill control system provided by Tenova I2S or another automation supplier. The systems are highly networked and provide a high degree of interface via an internationally standardised, onboard OPC server, allowing the system to interface seamlessly to a broad range of commercially available control and automation equipment and systems (including legacy systems via analog signal exchanges).

The STM system architecture is based on a partitioning, distribution and decentralisation of the overall gauging system’s control and measurement activities/responsibilities. The development of this architecture followed four primary objectives:

- Provide complete independent control of an individual C-frame system with a localised real-time controller.
- Provide immediate digitisation of the pre-amplifier’s analog signal with complete, calibrated real-time signal processed thickness measurement local to the C-frame, and provide only digital/numerical indications of the measured thickness from that point onward.
- Provide broad, networked, high-speed, numerical thickness measurement distribution, both within and external to the gauging system.
Finishing processes independently controlled and operated by a dedicated real-time controller. These local controllers function as standalone units, handling and supervising all aspects of the signal processing, control, operations and calibration (including the storage of all calibration data) of the measuring head and C-frame, along with rendering numerical/digital values of the measured thickness local to the C-frame. The controllers and associated support equipment reside in an environmentally protected enclosure, in direct proximity to an individual C-frame/measurement head. Figure 5 provides an illustration of this system arrangement and the partitioning between the real-time processor and FPGA hardware.

**FPGA hardware** This hardware is programmed to receive the digitised, pre-amplifier measurement of the detector’s sensor (from the A/D) and perform the selected digital signals processing (DSP) algorithms immediately to render a calibrated thickness measurement. The resulting measurement can be output as a high resolution analog signal (to support legacy systems) or passed to the real-time operating system (RTOS) for distribution over the dedicated thickness measurement network (DTMNet). The signal processing parameters/calibration co-efficients are provided by the RTOS and openly accessible via the OPC interface.

**Real-time CPU/RTOS** This processor is responsible for all C-frame equipment control and operational activities including: closed-loop C-frame motion control, high voltage power supply supervision, air wipe/purge systems, magazine and shutter control, calibration and standardisation and safety and protection systems. This processor manages all network interfaces and supports the OPC server interface. All calibration, alloy compensation and signal processing parameters are handled by this processor and distributed on the OPC interface to maximise the interface, remote control, performance monitoring and diagnostic support. It also employs advanced web-based technologies (AJAX, HTML, Java Scripts) to allow publishing of real-time graphical and status data to thin client HMI computers (running Internet Explorer, Firefox, Chrome, etc), and through directed Internet access (via the higher level systems), remote monitoring capabilities.

**DTMNet** This dedicated thickness measurement real-time, deterministic network (EtherCAT, etc) provides high-speed data exchanges (thickness indications and status broadcasts) between the gauging system and the AGC system (or another gauge monitoring, quality tracking system). In this way, the separation between equipment is not hampered by noise and interference experienced by long analog signal runs.

Support a wide variety of graphical user interfaces (GUIs) and associated commercially available HMI environments. Figure 4 provides a hierarchical description of the system’s network topology and the interconnection of the primary components.

The networked interconnections significantly reduce field wiring and allow the free-standing C-frame system to be conveniently integrated into broader industrial applications. The digital/numerical nature of the high-speed network data exchanges, eliminates the need for long analog signal runs and provides inherent noise immunity. The distance between system components (eg, C-frame system and operator interfaces/GUIs/HMIs) is limited only by the capabilities of the network media (copper wire, fibre optic, etc). This arrangement is completely scalable/expandable, through direct replication of the C-frame system and the attachment of additional HMI computers, as network drops.

The primary components are:

**Local C-frame controller** Each C-frame is
FORMING PROCESSES

**Fig 6** Layout diagram showing the system’s primary components, the potentially remote locations and the reduced field wiring requirements

**User interfacing** The highly networked nature of the system architecture and the C-frame controllers provide a number of opportunities for interfacing and scalability/expansion. The popularity of OPC server technologies allows extensive availability of the C-frame controller’s internal parameters, high voltage and detector calibration data, command and control structures, collected data buffers, performance and status data, etc. This broad and selectable exposure of OPC tags allows the C-frame controller to be easily integrated into complex automation systems and externally controlled/tuned to match the needs of the application and process.

The networked interfacing also gives a substantial reduction in the extent of field wiring required to support the overall thickness measurement system, and has a direct impact on the installation activities. Figure 6 shows the general system components and their associated interconnections.

**CONCLUSIONS**

Historically there has been a lack of commercially available hardware appropriately optimised for high-performance AGC/STM applications. The new COTS technologies-based FPGA hardware and multi-core processors offer the ability to implement the desired, optimised attributes of customised, proprietary hardware in the form of commercial, openly available, programmable hardware.

New processor and FPGA technologies have allowed advanced real-time control, signal processing and complex analytic compensation to be performed in locations previously not considered acceptable for computer/controller equipment (ie, local to the C-frame/measurement head). Highly networked, distributed architectures eliminate long analog signal runs, while offering broad interfacing and flexible scaling/expansion. Advanced web-based technologies coupled with OPC servers provide the ability to support highly interactive, fast responding GUIs via thin clients executing on general purpose HMI computers. Furthermore, these methods provide Internet accessibility for remote control, monitoring and diagnostic assistance from any access point, worldwide.

The new Tenova I2S AGC and STM system architectures and implementations have been conceived and developed with the end user and these difficult issues in mind. This new architecture has fulfilled our design/developmental goals, along with satisfying the performance and supply concerns of the end users. Many manufacturers of FPGA-based, general purpose equipment are introducing a broad spectrum of compatible hardware.

Programming the FPGA hardware using internationally standardised HDL allows these codes and algorithms to be seamlessly ported to other manufactures’ FPGAs. This offers an open market of commercially available boards and systems, all of which can be used interchangeably. This fact alone should alleviate any fears that this equipment has been made solely for some niche market – and may therefore become obsolete in short order.

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